Gate-Workfunction Engineering Using Poly-(Si,Ge) for High-Performance 0.18μm CMOS Technology

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Abstract

We show that poly-SiGe can be readily integrated as a gate material into an existing CMOS technology to achieve significant increase in the transistor performance. In order to preserve the standard salicidation scheme, a buffer poly-Si layer is introduced in the gate stack. PMOST channel profiles are optimized to account for the change of the gate workfunction. High-performance CMOS 0.18μm devices are manufactured using p- and n-type poly-Si/$Si_{0.8}Ge_{0.2}$ gates.

Introduction

With MOS transistors scaled down to deep submicron dimensions, short-channel effects and subthreshold leakage are becoming more difficult to control. The current drivability (I_{on}) can be improved by changing the channel profile to super-steep retrograde (SSR). This cannot solve, however, the problem of high subthreshold currents (I_{off}) due to low threshold voltage. An alternative approach is based on changing the gate workfunction. With modifying the gate-to-semiconductor workfunction difference $\Delta\Phi_{MS}$, one can change the channel doping while retaining the same V_T. We have recently reported [1] the use of poly-SiGe as a gate material where the $\Delta\Phi_{MS}$ for PMOSTs was tailored by the change in Ge mole fraction. Process compatibility with existing Si technology has been shown and significant improvements of deep-submicron PMOST performance have been observed.

We present here for the first time the results of the integration of such gates into a full 0.18μm CMOS processing flow. PMOST channel profiles have been numerically optimized for these "mid-gap" gates. "Stacked" two-layer gate structures were used: bottom poly-SiGe to control the gate workfunction and top poly-Si to employ a standard salicidation scheme. Excellent device parameters were obtained.

Process and device simulations

Figure 1 summarizes the impact of the Ge mole fraction change in the p-type poly-SiGe gate on the gate-semiconductor workfunction difference $\Delta\Phi_{MS}$ based on the data available from literature [2,4,6] and our experiments. There is only a negligible change for n-type poly-SiGe.

On the basis of process and device simulations calibrated to results in [1] we have performed an optimization analysis of

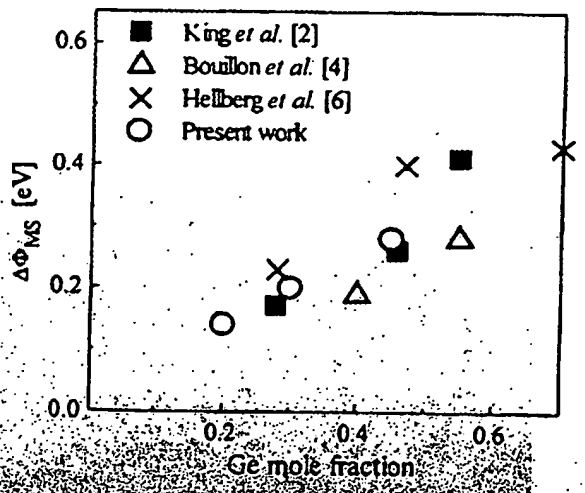

Figure 1: Summary of the p-type poly-SiGe-gate to n-type semiconductor workfunction difference $\Delta\Phi_{MS}$ dependence on the Ge mole fraction. In the present work the change in the Φ_{MS} is measured by the extrapolation of the flatband voltage to t_{ox}=0 [2].

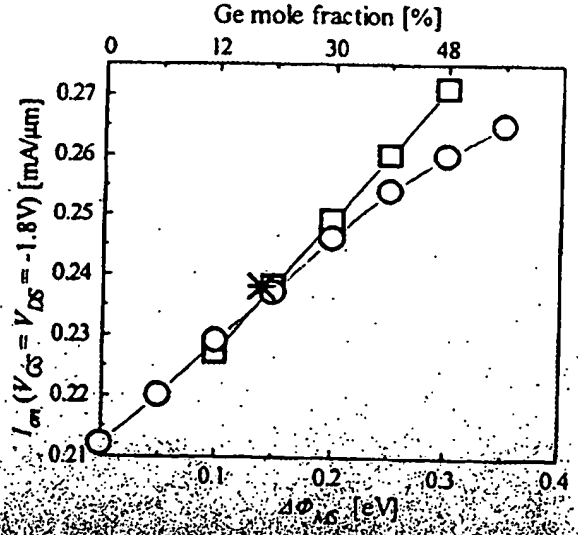

Figure 2: The results of the optimization analysis for the SSR well profile combined with poly-(Si,Ge) gate for 0.18μm PMOST. Dose and energy of SSR implant were optimized for the maximum I_{on} for two criteria: constant V_T=-0.3V (squares) or constant I_{off}~20pA/μm (circles). The star symbol represents the actual measured value.

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the SSR dose and energy matrix to obtain the highest current drive for a given V_T or I_{off} (see figure 2) for different Ge mole fractions for a 0.18μm PMOS device. A strong increase in the I_{on} as compared to standard poly-Si gates is predicted for the same I_{off} (up to 35% increase for 55%Ge). It is clear from the analysis that a significant improvement of the CMOS performance can be achieved, without any sacrifices for short-channel nor "off-state" behavior of the devices, by careful tuning of the gate workfunction and channel profile combination.

CMOS integration

A full integration of the poly-SiGe gates into the CMOS flow requires salicidation to reduce the gate and source/drain parasitic resistances and to ensure a good ohmic contact, if *n*- and *p*-type gates are used for NMOS and PMOS transistors respectively. It is known, however, that the reaction of Ti with poly-SiGe drastically differs from that of Ti with poly-Si [3]. To elevate this problem we use a "stacked-gate" structure consisting of two layers: bottom poly-SiGe to control $\Delta\Phi_{ms}$ and top poly-Si to retain the standard salicidation scheme.

Apart from the gate formation trajectory, all other processing steps of the full 0.18μm CMOS flow have been reproduced featuring 4.5nm-thick gate oxide (determined from C-V measurements), e-beam gate lithography, HDD source/drain low-energy implantations, Ti salicidation, planarization and a single metal level. In figure 3 we present the cross-section of the active part of a completed 0.18μm device, with the gate consisting of the 50nm bottom poly-$Si_{0.7}Ge_{0.3}$ layer and 100nm poly-Si on top (as deposited). The use of stacked structures does not amount to any additional complications concerning etching or sidewall re-oxidation. The use of a buffer poly-Si layer creates, however, another issue addressed in the next two figures: during the post-gate-processing, Ge atoms from the bottom layer diffuse upwards into the poly-Si thus reducing the Ge content in the bottom layer (figure 4). The final Ge mole fraction determines $\Delta\Phi_{ms}$ and should be monitored. Once measured for a given thermal budget, it can

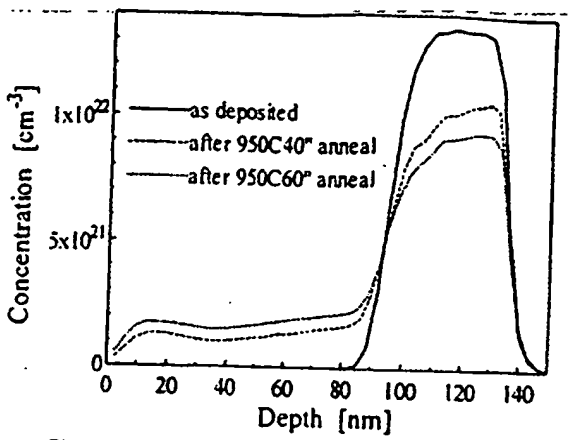

Figure 4 SIMS profiles of Ge diffusion from the bottom poly-SiGe (50nm, 27% Ge as deposited) layer into the top poly-Si (90nm) layer during processing. Values are normalized to the Rutherford back-scattering measurements. A linear scale is used for the vertical axis.

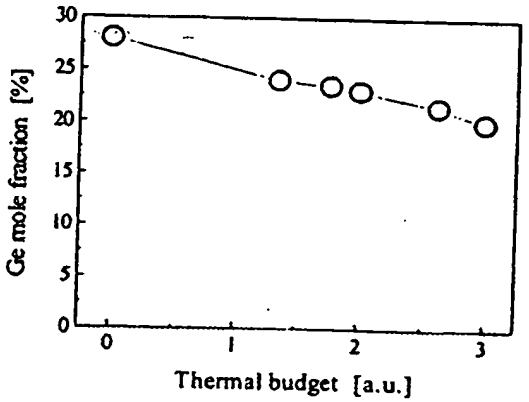

Figure 5 A reduction in the Ge mole fraction in the bottom layer of the stacked gates with an increase in a thermal budget.

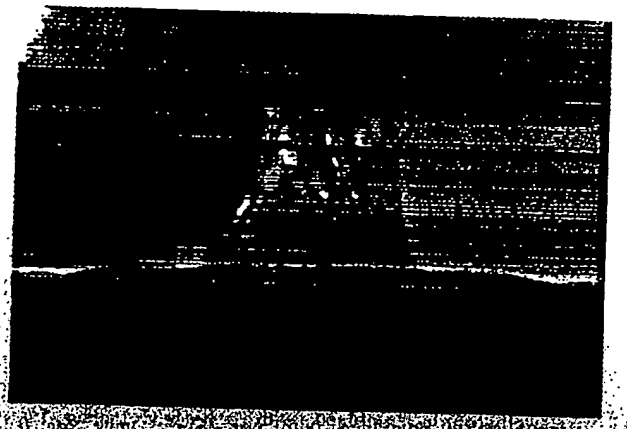

Figure 3 TEM cross-section view of the completed stacked 0.18μm gate with bottom 50nm poly-$Si_{0.7}Ge_{0.3}$ layer and top 100nm poly-Si layer.

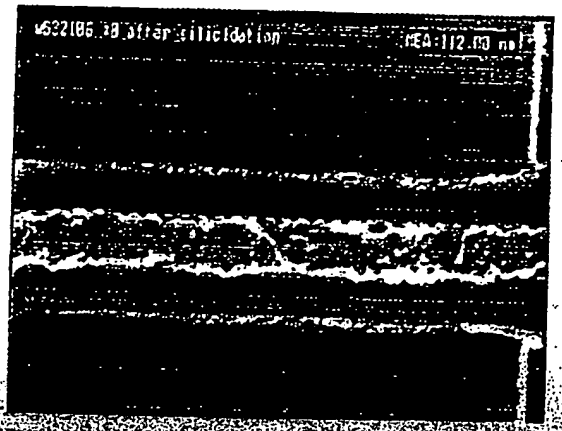

Figure 6 SEM top view of a 0.1μm poly-Si/SiGe gate and source/drain regions after self-aligned Ti silicidation. 100nm-thick oxide spacers are used to separate the regions.

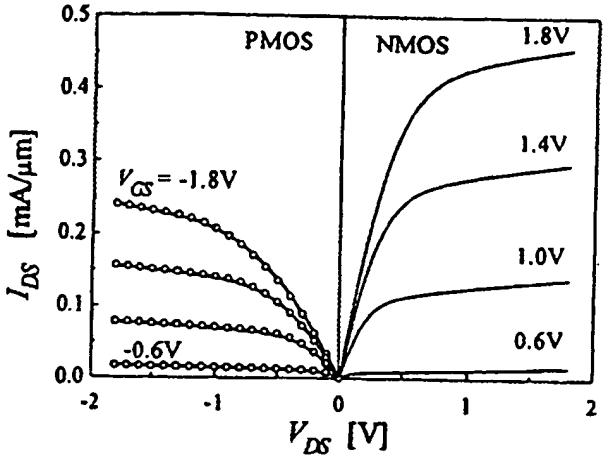

Figure 7 Typical I_{DS}-V_{DS} characteristics of NMOS and PMOS transistors with L_{drawn} = 0.18μm with poly-Si/$Si_{0.8}Ge_{0.2}$ gates. Open symbols for PMOST data are the results of numerical simulations.

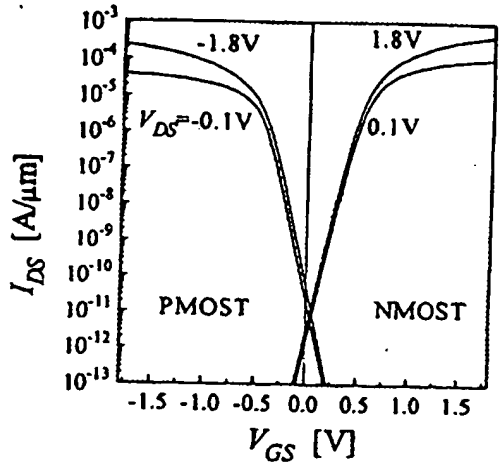

Figure 8 Typical subthreshold characteristics of NMOS and PMOS transistors with poly-Si/ $Si_{0.8}Ge_{0.2}$ gates. L_{drawn} =0.18μm.

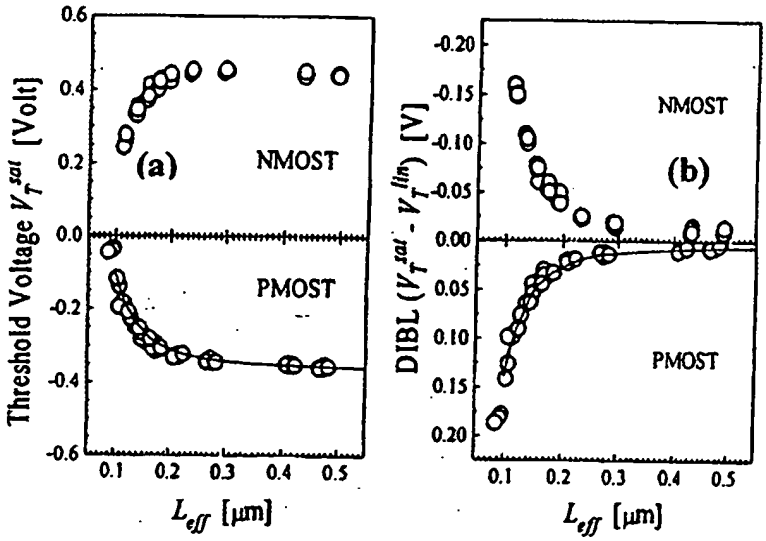

Figure 9 Saturation V_T (V_{DS}=-1.8V) (a) and DIBL (b) for NMOS and PMOS transistors with poly-Si/$Si_{0.8}Ge_{0.2}$ gates. Solid lines for PMOST data are the results of numerical simulations assuming $\Delta\Phi_{ms}$ = 0.14eV.

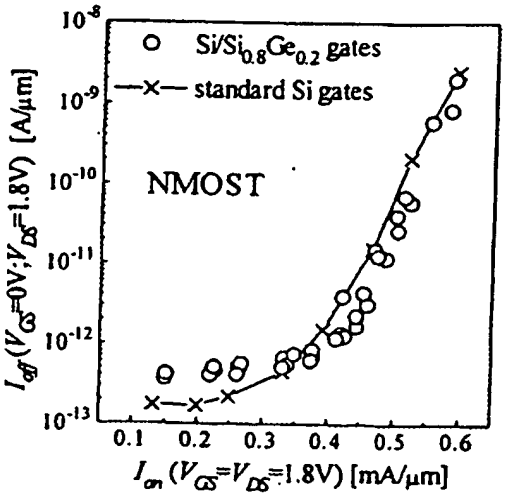

Figure 10 Current drive against leakage currents for NMOS devices with poly-Si/$Si_{0.8}Ge_{0.2}$ gates compared to the standard poly-Si gated transistors values. The CMOS processing with poly-Si/SiGe gates shows as good I_{off}/I_{on} ratios as in the standard technology.

be used in the consequent device designs (figure 5). *Ge* up-diffusion into the top layer (amounting to ~3%) does not influence the salicidation process: figure 6 shows the SEM micrograph of the results of Ti salicidation of a 0.11μm gate. The sheet resistances after salicidation of the gate and source/drain are 15.4 Ω/□ (6.6 Ω/□) and 14.6 Ω/□ (4.5 Ω/□) for NMOS (PMOS) transistors respectively (as measured on 0.3μm-wide structures).

Electrical results

We present here the results obtained with the poly-Si/$Si_{0.8}Ge_{0.2}$ gates with Ge mole fraction confirmed from the RBS measurements after full processing. The diffusion and electrical activation of the dopants in *p*-type poly-SiGe is superior to the standard poly-Si gates [1], resulting in better gate activation and minimal de-activation (less than 10% gate depletion after full processing as deduced from the *C-V* measurements).

Typical *I-V* curves of the transistors with poly-Si/$Si_{0.8}Ge_{0.2}$ gates with L_{drawn} = 0.18μm are presented in figures 7 and 8. In sub-V_T region excellent voltage swing values of 80mV/dec (PMOST) and 78mV/dec (NMOST) are obtained insuring a low level of "off"-state leakage currents (50pA/μm and 5pA/μm respectively). The maximum saturation currents for these devices are: 240 μA/μm (PMOST) and 455 μA/μm (NMOST). High R_s (0.42) and small ΔL (~10nm for NMOST and 30nm for PMOSTs) are responsible for somewhat lower values of I_{DS}^{sat} for NMOST. At the same time, NMOST I_{on}/I_{off} ratios are on the level of the best values reported [5] (see

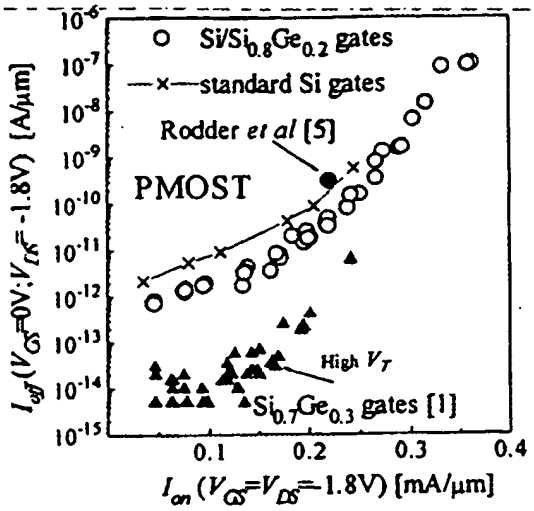

Figure 11 Current drive against leakage currents for PMOS devices with poly-Si/$Si_{0.8}Ge_{0.2}$ gates compared to the standard poly-Si gate transistors and the previously reported values for PMOS-only processing with poly-$Si_{0.7}Ge_{0.3}$ gates. Both variants with poly-SiGe gates compare favorably to [5].

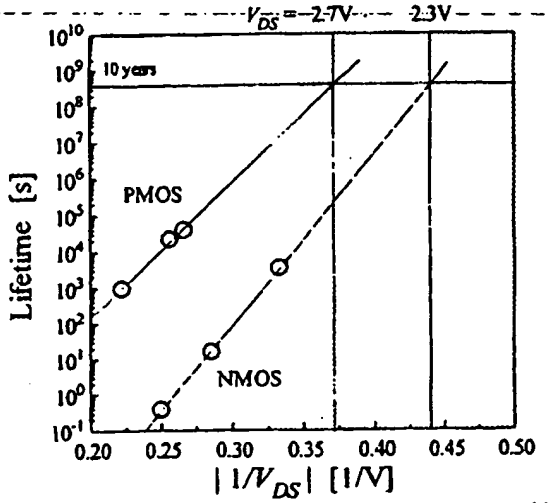

Figure 12 Lifetime of the MOS transistors with gate oxide stressed under the worst scenarios. Based on the hot carrier degradation measurements where failure is detected when the transconductance changes by 10% under continuous stress. The manufactured devices can be safely operated for 10 years at V_{DD} higher than 1.8V (up to 2.3V for NMOST and 2.7V for PMOST) to result in increased current drivability of the circuits.

figures 10 and 11). A careful channel profile engineering (SSR well profile, localized pocket implants around source/drain) insures that the short channel effects are well-controlled (figure 9) down to L_{eff}=0.12μm. In figure 10 the current drive (I_{on}) of the NMOST is plotted for standard (poly-Si gates) and new (poly-Si/$Si_{0.8}Ge_{0.2}$ gates) technologies showing, as expected, the same behavior. On the other hand, there is a ~15% improvement in PMOST performance (figure 11). Numerical simulations are in excellent agreement with the experimental results (see figures 2, 7 and 9). Our PMOS devices also compare favorably to those reported in [5].

The results of the hot-carrier degradation of the transistor performance with poly-Si/$Si_{0.8}Ge_{0.2}$ gates are presented in figure 12. Here, a maximum substrate current condition was used for NMOS transistors and $V_{GS} \cong 1/2(V_{DS})$ for PMOSTs, both being the worst stress conditions for respective device. For a supply voltage of 1.8V, the device lifetime is well beyond the 10-year limit that is conventionally used to characterize the long-term reliability of the process.

To demonstrate the capability of the manufactured devices to be integrated in to a CMOS circuit we show in figure 13 a typical waveform of the 51-stage unloaded CMOS inverter.

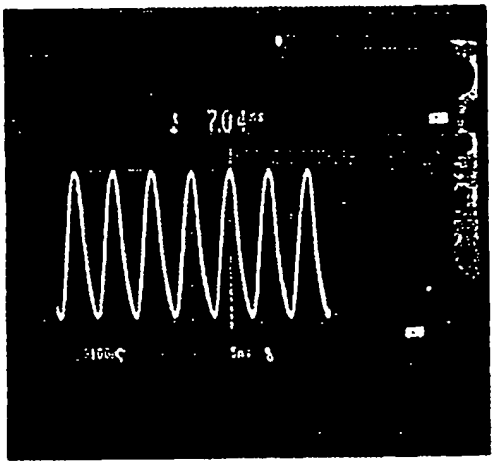

Figure 13 A waveform of the unloaded 51-stage CMOS ring oscillator. V_{DD} = 1.8V.

Conclusions

We have shown that poly-SiGe can be readily integrated as a gate material into an existing CMOS processing flow. The change in the Ge mole fraction controls the change in the gate-semiconductor workfunction difference which, coupled to a channel profile tuning, can result in a significant improvement of the PMOST performance. High-performance CMOS 0.18μm devices have been manufactured using p^+- and n^+-type poly-Si/$Si_{0.8}Ge_{0.2}$ stacked gates.

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